Notice of Allowability	Application No.	Applicant(s)	
	09/977,994	NAGATA ET AL.	
	Examiner	Art Unit	
	Jeffrey R. West	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the Appeal Brief filed 24 August 2005*.

2. ☒ The allowed claim(s) is/are *1-14*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Allowable Subject Matter

1. Claims 1-14 are considered to be allowable over the cited prior art for the following reasons:

Nagata et al., "Measurements and Analyses of Substrate Noise Waveform in Mixed Signal IC Environment" discloses a method for performing measurements and analyses of substrate noise waveform in mixed signal integrated circuit environment comprising representing the integrated circuit according to a distribution of switching operations of a plurality of logic gates and a time series of statically-charged parasitic capacitors connected between a source line and a ground line (page 577, column 1, paragraph 5 and Figure 7). Nagata then discloses generating an analysis module by coupling one end of the group of capacitors with a parasitic impedance of the source line, and connecting the other end of the group of capacitors with a parasitic impedance of the ground line (Figure 7). Nagata also discloses that the source current from the analysis model along with the parasitic impedances of the source and ground lines causes a voltage variation, regarded as substrate noise (page 576, column 1, paragraph 3, page 577, column 1, paragraph 4, and Figure 5). Nagata further discloses that a value for the parasitic capacitances is determined every predetermined time interval wherein the time interval is set according to the switching operations of the logic gates (page 577, column 2, paragraph 2 to page 578, column 2, paragraph 2).

Nagata discloses assigning the group of parasitic capacitors to a group of logic gates wherein the digital circuit is divided into a plurality of segments along the border at which the parasitic impedances of the source line and the ground line are locally appended (i.e. increased) (Figures 7a-c and page 577, column 2, paragraph 2).

Nagata discloses that the capacitor groups are charged at a specific timing according to the output of a truth table (page 577, column 1, paragraph 5) wherein capacitance of the parasitic capacitor to be charged at a specific timing is calculated from input and output capacitance of the logic gates in the digital circuit to be analyzed (page 577, column 2, paragraph 2 and equation (2)) (input capacitances, $C_{ln,i}$ and $C_{lp,j}$, and output capacitances $C_{jn,i}$ and $C_{jp,j}$).

Nagata also discloses that the logical transitions correspond to the charging and discharging of all of the parasitic capacitors (i.e. charging of each parasitic capacitor in each group) (page 577, column 1, paragraph 5) and these logical transitions occur at different times in accordance with a predetermined time interval (page 578, column 1, paragraph 4 to page 578, column 2, paragraph 1).

U.S. Patent Application Publication No. 2002/0022951 to Heijningen et al. teaches a method, apparatus and computer program product for determination of noise in mixed signal systems caused by the switching operation of logic gates on a substrate (0007-0008) including representing the logic gate switching as capacitor groups in the form of a cell (0088, lines 1-5) and determining the noise as a source

current waveform (0089) wherein determining the power supply noise requires determining a capacitance contribution for each cell (i.e. capacitor group) independently (0119) and combining the individual waveforms to determine the total noise waveform (0127).

Mitra et al., "Substrate-Aware Mixed Signal Macrocell Placement in WRIGHT" teaches a computer-implemented method for handing substrate-coupled switching noise in a typical IC containing both sensitive analog and noisy digital circuits (abstract) comprising first receiving minimal area and wire length design specifications, designing the circuits based on the design specifications, and from the design determining the current substrate noise. Mitra then teaches re-designing, based on the substrate noise results, the circuits and guard ring/band positions to obtain acceptable substrate noise results (page 275, column 2, paragraph 3 to page 276, column 1, paragraph 3).

As noted above, the cited prior art teaches many of the features of the claimed invention and while the cited prior art does teach analysis of a substrate noise waveform in a mixed-signal IC environment, none of the cited prior art teaches or suggests, in combination with the other claimed limitations for analyzing a waveform of a source current in a semiconductor integrated circuit including a digital circuit having a plurality of logic gates, generating an analysis model of the digital circuit with respect to a distribution of switching operations of the logic gates by coupling

one end of a time-division group of parasitic capacitors, one end of a group of parasitic capacitors charged statically, and parasitic impedance of a source line; connecting the other end of the time-division group of parasitic capacitors, the other end of the group of parasitic capacitors charged statically, and parasitic impedance of a ground line; and determining a waveform of the source current in the digital circuit from the analysis model, wherein a time-division group of capacitors is specifically defined as illustrated in Figure 2c.

The following newly cited references are also considered to be pertinent to the examination of the instant application but also fail to teach or suggest, in combination with the other claimed limitations for analyzing a waveform of a source current in a semiconductor integrated circuit including a digital circuit having a plurality of logic gates, generating an analysis model of the digital circuit with respect to a distribution of switching operations of the logic gates by coupling one end of a time-division group of parasitic capacitors, one end of a group of parasitic capacitors charged statically, and parasitic impedance of a source line; connecting the other end of the time-division group of parasitic capacitors, the other end of the group of parasitic capacitors charged statically, and parasitic impedance of a ground line; and determining a waveform of the source current in the digital circuit from the analysis model, wherein a time-division group of capacitors is specifically defined as illustrated in Figure 2c:

Su et al., "Experimental Results and Modeling Techniques for Substrate Noise in Mixed-Signal Integrated Circuits" teaches methods for modeling substrate noise.

Mitra et al., "A Methodology for Rapid Estimation of Substrate-Coupled Switching Noise" teaches methods for estimating switching noise in mixed-signal chips.

Charbon et al., "Modeling Digital Substrate Noise Injection in Mixed-Signal IC's" teaches techniques for modeling substrate noise.

U.S. Patent No. 5,481,484 to Ogawa et al. teaches a mixed mode simulation method and simulator.

U.S. Patent No. 6,144,217 to Iwata et al. teaches a low switching noise logic circuit.

U.S. Patent No. 6,732,065 to Muddu teaches noise estimation for coupled RC interconnects in deep submicron integrated circuits.

U.S. Patent No. 6,618,837 to Zhang et al. teaches MOSFET modeling for IC design accurate for high frequencies.

U.S. Patent No. 6,564,355 to Smith et al. teaches a system and method for analyzing simultaneous switching noise.

U.S. Patent No. 6,480,986 to Richer teaches IC substrate noise modeling including extracted capacitance for improved accuracy.

U.S. Patent No. 6,397,172 to Gurney teaches adaptive integrated circuit design simulation transistor modeling and evaluation.

U.S. Patent Application Publication No. 2003/0125919 to Chikamichi teaches circuit modeling using topologically equivalent models.

2. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey R. West whose telephone number is (571)272-2226. The examiner can normally be reached on Monday through Friday, 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (571)272-2216. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jrw
November 28, 2005

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